A SIMPLE COMPUTER FOR FOURIER ANALYSIS AND SYNTHESIS

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(*Received February 7, 1964*)

ABSTRACT. Three methods of computing Fourier coefficients by simple circuitry have been investigated. In the two Digital Schemes for evaluating Σf_j Cos θ_j or Σf_j Sin θ_j the Sine/Cosine translator is a selecting-cum-marker circuit using either two-motion electromechanical switches or diode matrices. The translated digits Cos θ_j/Sin θ_j are read out in the form of pulses, each of which again generates f_j pulses by triggering preset multivibrators. The sum is then obtained by counting all the serial pulses in a reversible counter. The translator is further simplified in a Hybrid computer, where analogue voltages proportional to Cos θ_j/Sin θ_j and f_j are multiplied in a semi-digital form, and the output is again in the form of a number of pulses proportional to the product. These methods are easily extended to two- and three-dimensional problems. An accuracy of 1% or better is easily obtained in the Hybrid computer, and the speed of operation, normally about 500 per hour, depends on the input circuits feeding θ_j and f_j.

INTRODUCTION

Many applications of Fourier Series and Fourier integrals are found in all branches of science and engineering, and in most practical cases, numerical methods have to be used to evaluate the Fourier coefficients. A periodic function $f(\theta)$ may be represented as,

$$f(\theta) = a_0+\Sigma a_n \cos n\theta+\Sigma\, b_n \sin n\theta$$

where,
$$a_0 = \frac{1}{2\pi}\int_0^{2\pi} f(\theta)\cdot d\theta; \quad a_n = \frac{1}{\pi}\int_0^{2\pi} f(\theta)\cdot \cos n\theta \cdot d\theta;$$

and
$$b_n = \frac{1}{\pi}\int_0^{2\pi} f(\theta)\cdot \sin n\theta\cdot d\theta.$$

When $f(\theta)$ cannot be expressed in an analytic form, the above integrals are replaced by equivalent summations for numerical computation. Thus, either the synthesis of $f(\theta)$ from the given a's and b's, or the analysis of $f(\theta)$ in terms of the a's and b's require the determination of the sum of a series of the form $\Sigma f_j \cos \theta_j$ or $\Sigma\, f_j \sin \theta_j$.

Many mechanical, electromechanical and electrical instruments, viz., Harvey Harmonic Analyser, Cathode ray tube, Wave analyser, Spectrum analyser etc. (Manley, 1945), have been developed to aid this numerical computation. The problem may also be solved very accurately in a general purpose Digital computer, but such a machine is not available to all workers. It has been the purpose of the work, reported here, to solve the problem with much simpler circuits, but at the same time retaining some of the advantages of modern digital and analogue techniques.

PRINCIPLES OF COMPUTATION

The main problem in Fourier analysis or synthesis is to numerically determine the summation $\Sigma f_j \cos \theta_j$ or $\Sigma f_j \sin \theta_j$ for various values of f_j and θ_j. The problem, then, consists of three parts, viz., (a) Determination of Cos θ_j/sin θ_j by some method of translation, (b) Multiplication of cos θ_j/sin θ_j by f_j, (c) Summation of the series, as indicated in Fig. 1. These functions may be done either by digital

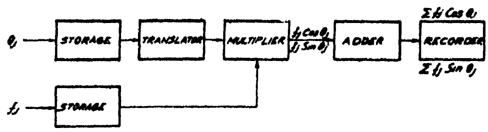

Fig. 1. *Block Schematic of the Computer.*

or analogue devices. The digital translator may be of electromechanical or electronic type. The input to the system may be stored by positioning some two-motion switches, and the translated digits may be retransmitted by impulse senders according to preset codes as is used in the Directors of a large automatic exchange. (Atkinson, 1955). The preset code may be changed, when required, by some rearrangements in the Translation field only. Using 3-digit values of θ_j, the translated 3-digit values of cos θ_j/sinθ_j are transmitted to the multiplier in a serial order as shown in Fig. 2. To make the translator faster, electronic

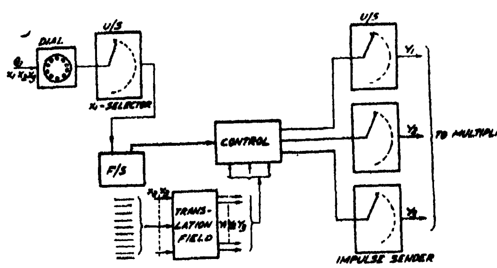

Fig. 2. *Translator using Electro-mechanical switches.*

circuits analogous to the above may also be used. Fig. 3 shows such a circuit, where the digits of θ are stored either in a bank of decade counters using dekatron

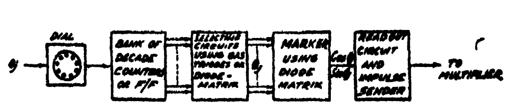

Fig. 3. *Digital translator using electronic devices.*

tubes or in flip-flops. The marked leads of the counters operate a selecting circuit and one output lead is energised. This in turn will mark the corresponding output leads of the marker matrix equivalent to the translator, and the marked leads will indicate the value of $\cos\theta_j/\sin\theta_j$. The selecting and marker matrices may be designed with either cold-cathode gas-discharge tubes or diodes (Flowers, 1952), and the impulse senders may be preset triggered-multivibrators giving a set number of pulses corresponding to $\cos\theta_j/\sin\theta_j$.

The analogue translator may be a Diode-function generator or a survosystem using sine/cosine potentiometers. A simpler analogue sine/cosine function generator has been developed using the sampling technique, as seen in Fig. 4. Here θ_j is represented by a variable voltage which in turn varies the position of a

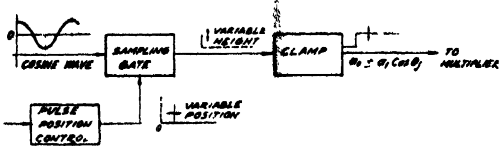

Fig. 4. *Analogue translator using Sampling techniques.*

sampling pulse with reference to the zero of a sinusoidal wave fed to the sampling gate. The sampled value will correspond to $\sin\theta_j/\cos\theta_j$ and is transferred to the multiplier through a suitable clamp.

Since in simple calculations, a 2-digit or 3-digit accuracy in $\cos\theta_j/\sin\theta_j$ and f_j would be sufficient, it is not necessary to use the complicated multiplying circuits required in standard digital computers. The serial pulses obtained from the translator-sender may be multiplied sequentially by generating a preset number of pulses corresponding to f_j for each pulse of $\cos\theta_j/\sin\theta_j$. The total number of pulses, if counted, would represent $f_j\cos\theta_j/f_j\sin\theta_j$. This may be accomplished by presetting the triggered multivibrators with f_j and by allowing the MV's to be triggered once for each input pulse representing $\cos\theta_j/\sin\theta_j$, as shown in Fig. 5.

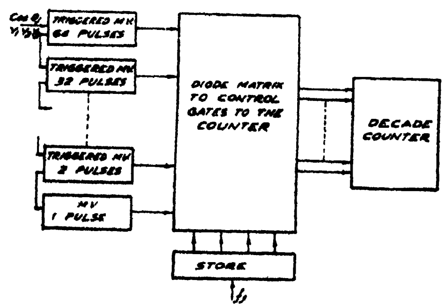

Fig. 5. *Digital multiplier.*

Here the inputs $y_1\,y_2\,y_3$ trigger a series of MV's which are controlled by auxiliary counters to produce a predetermined number of pulses according to the Binary code. The output from the MV's are then controlled by a diode matrix preset by the codes of f_j and only those MV's which combine to form the number in f_j are allowed to transmit their pulses to the final counter. Thus each pulse in $y_1\,y_2\,y_3$ will send f_j pulses to the counter. Instead of using Binary-coded triggered

MV's, we may also use auxiliary decade counters in the feedback loop of the *MV*'s so as to control the number of pulses given by them and the counters would be preset by the digits in f_j.

Many types of analogue multiplics are in use, e.g., the multiplier using simultaneous amplitude and width modulation of sampling pulses, the multiplier using amplitude and frequency modulation of a sinusoidal carrier (Aiken and Susskind, 1961). The latter method is quite simple in circuitry and the *FM*-discriminator may be either a special network having the required slope-frequency characteristic (Tuttle, 1953) or a standard Foster-Seely circuit. The circuit may be further simplified by using a frequency-controlled *MV* as the carrier to the *AM*-modulator and the output simply detected by a diode and an *RC*-filter. This method, shown in Fig. 6., has the defect that the output is not simply e_1e_2; but has some constants

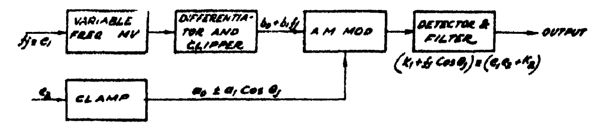

Fig. 6. *Analogue multiplier.*

K_1 and K_2 varying with f_j and cos θ_j., and would require cancellation by suitable variable voltages. The problem has been effectively and simply solved by the Frequency-Counting multiplier shown in Fig. 7, where f_j controls a gate circuit with

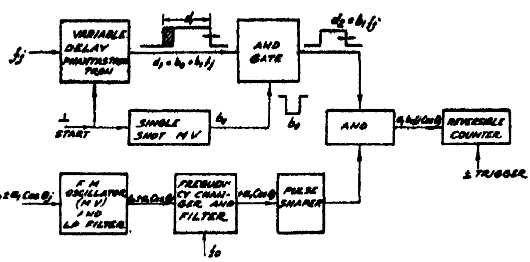

Fig. 7. *Frequency counting multiplier.*

a pulse of variable width $= b_1 f_j$ and pulses corresponding to a_1 cosθ_j are passed through the gate. The number of the output pulses is then proportional to $a_1 b_1$ f_j cos θ_j, which are finally counted. The method has the added advantage that by using reversible counters (Churchill, 1952), $\pm$ sign of cosθ_j may be taken care of by making the counter to add or to subtract in response to a trigger from the translator. The summation of the series Σf_j cos θ_j is done most conveniently by digital methods using either a Binary or a Decade counter, and standard circuits are used for the pupose (Lesslie and Narin, 1962).

DIGITAL SCHEMES

Based on the principles of Figs. 2 and 5, an electromechanical digital computer is shown in Fig. 8, where the values of θ_j and f_j are assumed to be of two digits each. The circuits may be easily extended for more digits in θ_j and f_j. The dialled digit $X_1 X_2$ of θ_j drive a two-motion selector switch, similar to a Final selector in an auto-exchange (Atkinson, 1955), and mark a particular contact on the P-bank with full earth. All the contacts of the P-bank are connected to the

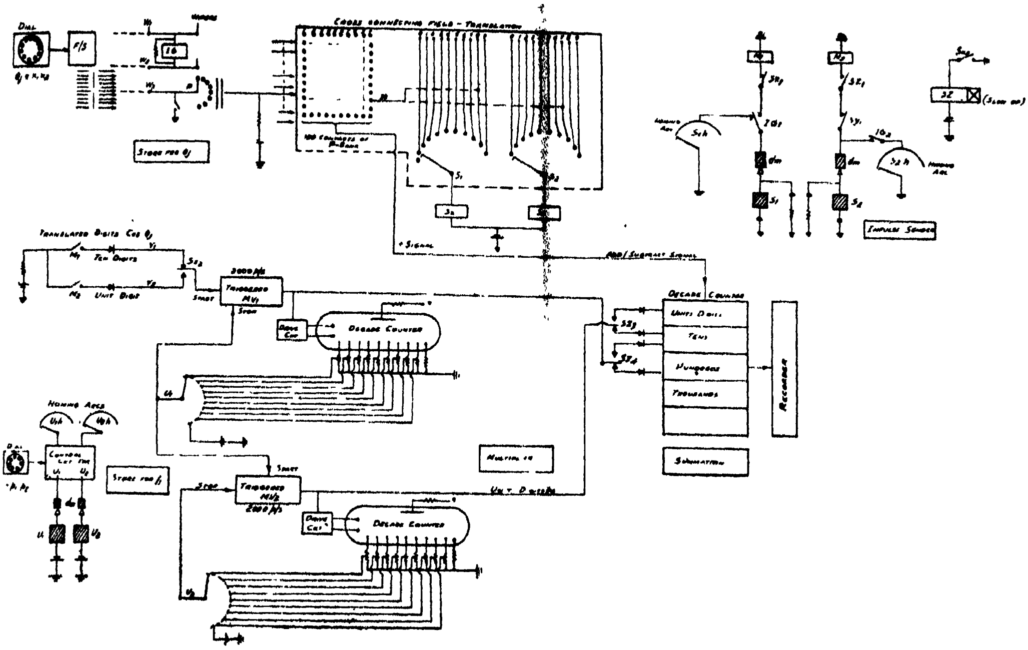

Fig. 8. A Complete Electro-mechanical Computer. (Translator connection shown for Cos 30° = 0.87).

Translation field such that $X_1 X_2$ ultimately earth a pair of predetermined vertical wires connected to the outlets of S_1 and S_2 (e.g., for $\theta_j = 30°$, the wires 8 and 7 are earthed as shown in the figure)). Along with the selection of Cos θ_j, the other wipers of the selector operate the relay IG and IG_1 starts the uniselector magnet S_1, which hunts through its own interrupter contact for the earthed wire (say, no. 8 in the Fig.). When the wiper S_1 reaches the marked wire, the U/SS_1 stops due to the operation of SX and U/S S_2 starts hunting due to the operation SZ. S_2 in its turn stops when the marked wire is encountered by the wiper S_2 The uniselectors are brought back to normal by the homing arcs S_{1h} and S_{2h} when IG is released. During the impulsing of S_1 and S_2, the relays M_1 and M_2 send the translated digits $Y_1 Y_2$ in a sequence and the pulses actuate the triggered multi-vibrator MV_1 repeatedly. The multivibrators MV_1 and MV_2 are preset by the dialled digits $p_1 p_2$ corresponding to f_j so that each pulse due to M_1 and M_2 produces (p_1+p_2) pulses at the output of the MV's, and the final decade counter counts and stores them. The dialled pulses $p_1 p_2$ actuate two U/S's U_1 and U_2 and position their wippers accordingly to control the number of pulses sent out by MV_1 and MV_2 each time they are excited by Y_1 or Y_2. This is done by counting the output pulses by an auxiliary decado counter using Dekatron tubes (or flip-flops), and stopping the MV when the marked cathode sends a stop pulse back to the MV. The stop pulse via U_1 for MV_1 starts MV_2 and finally MV_2 stops due to a stop pulse via U_2 from its own counter. Due to the controlling contacts SZ_2, SZ_3 and SZ_4, the pulses $Y_1\,p_1$ are fed to the Hundreds' position and the pulses $Y_1\,p_2$ to the Tens' position of the counter. Similarly the pulses $Y_2\,p_1$ and $Y_2\,p_2$ are fed to the Ten's and Unit's positions respectively. The ambiguity of $\pm Y_1 Y_2$ for $\cos\theta_j$; may be taken care of by using a reversible counter (Churchill, 1952) for the final summation. In Dekatrons, reversing the drive changes the direction of rotation of the glow and addition or subtraction may be done by simply changing the drive circuit. To affect this addition or subtraction, a control signal is obtained form the translation field and either the direct or reverse drive circuit is used to store the digits $Y_1\,p_1$, $Y_2\,p_1$, $Y_1\,p_2$ and $Y_2 p_2$. Thus $(\pm Y_1\ Y_2 \times f_j) = f_j \cos\theta_j$; pulses are effectively stored in the final counter. The selector circuits may be released by an auxiliary contact in the dial and the operations repeated in a serial manner.

For an accuracy of two decimal places for θ_j and f_j, one two-motion selector, four uniselectors along with the auxiliary circuits and final counters would be required. Since the U/S's normally can give about 50 pulses per second and dialling requires about 2 seconds per digit, it will be possible to do about 350 summing operations in an hour if one can dial that quickly. The speed of MV's would be about 2000 pulses/second as it is necessary to send at most 20 pulses to the counter for each pulse due to M_1 or M_2. For three digit values of θ_j anf f_j, ten two-motion selectors and seven U/S's would be necessary. The values of $\Sigma f_j \cos\theta_j$ may be recorded (Das, 1959) if required by a 'readout' circuit and an electrical typewriter at the output of the final counter.

All-electronic digital computer

It is possible to replace the electromechanical storage and the selecting circuits of the above scheme with all-electronic circuits, as shown in Figs. 3 and 9. Here the dialled digits $X_1\,X_2$ for θ_j are stored in a sequence in the ring counter M_1 and M_2 which are sequentially gated by the cold-cathode trigger tubes T_1 and T_2 (Flowers, 1951). The outputs of M_1 and M_2 control a diode-matrix D_1 so that a single output of the matrix is energised and the translated Cos θ_j ; is represented by an output $Y_1\ Y_2$ of the cross-connecting field. This output, in conjunction with the feed-back from the auxiliary counters M_3 and M_4, causes the marker matrix D_2 to send stop pulses to multivibrators MV_1 and MV_2, which are initially triggered by a start signal from T_3 synchronised with the translation of $X_1\,X_2$ to $Y_1\ Y_2$. Thus MV_1 and MV_2., controlled by these start-stop signals, transmit the translated digits $Y_1\ Y_2$ in a serial form to the multiplier unit. The ring counters M_1, M_2, M_3 and M_4 are reset before the new values of $X_1\ X_2$ are fed to the transalator.

The multiplier unit is similar to that of Fig. 8, and the ring counters M_5 and M_6 are preset by the dialled digits $p_1\,p_2$ corresponding to f_j. The pulses of $Y_1\ Y_2$ repeatedly triggers MV_3 (p.r.f. approx. 20 times that of MV_1) which sends out (p_1+p_2) pulses to the counter for each input pulse. It is possible to use the same MV_3 to send out p_1 and p_2 pulses if the reversible ring counters (Dekatron) M_5 and M_6 are preset by p_1 and p_2 through direct drive circuits (equivalent to addition) and are reset by the pulses from MV_3 through reverse drive circuits

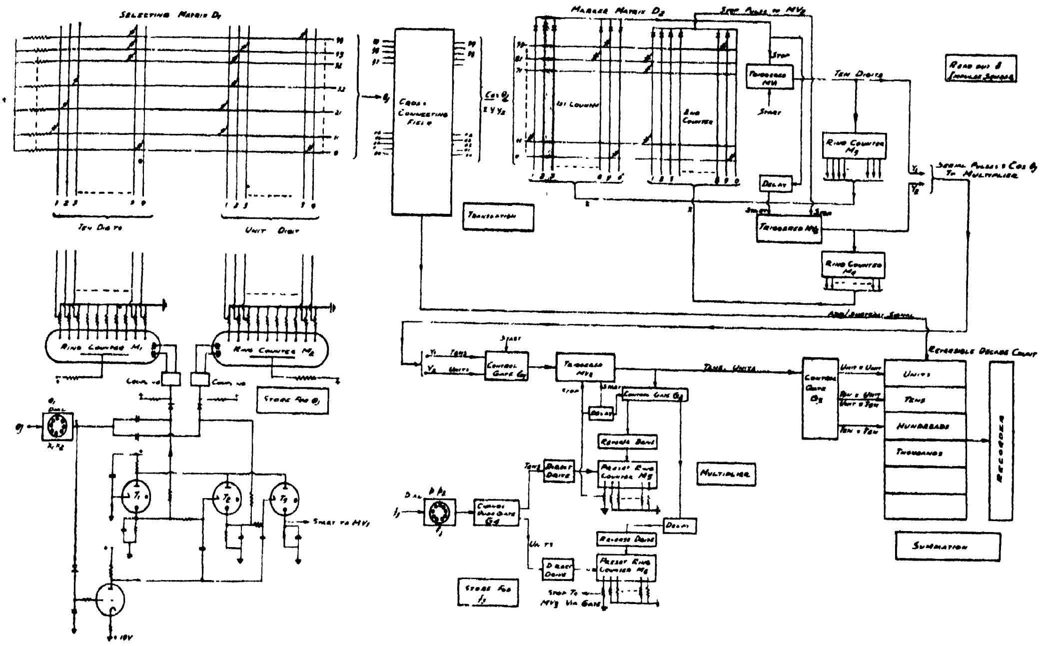

Fig. 9. An all-electronic Digital Compute..

(equivalent to subtraction) so that the stop pulses are always generated at the first cathodes of M_5 and M_6. The counters M_5 and M_6 are controlled by the gate G_2 to allow their operation in a sequence, and the gates G_1, G_2 and G_3 are synchronised so that proper inputs are fed to the final counter in proper sequences i.e. Y_1 p_1 to the Hundreds' position, Y_1 p_2 to the Ten's position etc. The final counter is a reversible one, as explained in section 3, and the addition/subtraction is controlled by a signal from the translation field.

The circuit of Fig. 9 is for two-digit values of θ_j and f_j and may be extended to three or four digit-values by using additional counters and larger diode matrices. For two-digit values, approximately ten decade counters and 500 diodes with their associated control circuits would be required. For 3-digit values, 13 counters and 700 diodes would be necessary. For Dekatron counters, the speed of counting is about 4-20 thousand pulses per second, but using hard valve circuits, higher speed of counting may be obtained. Thus the number of summing operations that can be performed in an hour mainly depends on the input circuits feeding the values of θ_j and f_j. With dialled inputs, about 8 seconds would be required to feed the digits and not more than 500 operations can be done in an hour. The speed of operations may be improved by feeding the digits through punched tapes or such other faster devices.

A HYBRID COMPUTER

The principles of a hybrid computer has been shown in Figs. 4 and 7. A complete block schematic of the computer, along with the different timing waveforms, is shown in Fig. 10. The inputs θ_j and f_j are in the form of calibrated voltages

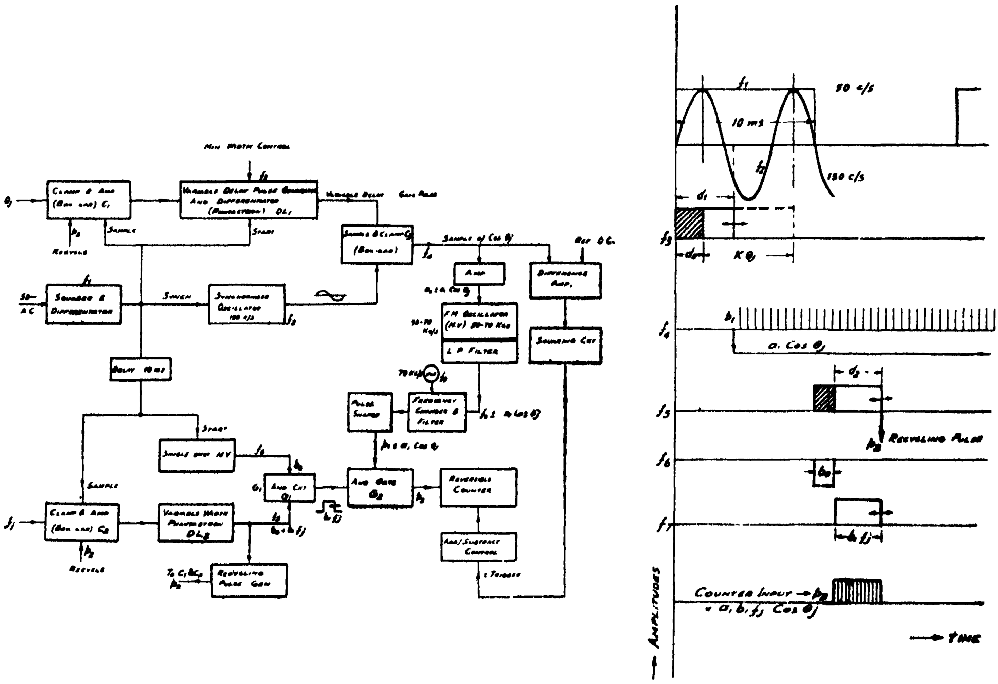

Fig. 10. *An all-electronic Hybrid computer.* (a) Block Schematic of the equipment. (b) The Timing waveforms of different circuits.

which are clamped by the 'Boxcar' circuits C_1 and C_2.The variable delay generators DL_1 and DL_2 are Phantastrons with controllable mean delay so that the Sine/Cosine wave form f_2 and the delayed pulses f_3, f_4 and f_5 are properly synchronised. The translation of θ_j to cos θ_j is obtained by the combined operations of the 'Boxcar' C_3, *FM* oscillator and frequency changer, and the pulses p_1 is proportional to cos θ_j. The width of the gate pulse f_7 is controlled by f_j and the output of the gate G_2 is $a_1 b_1 f_j \cos\theta_j = p_3$ pulses which are counted and stored in the final reversible counter.

The characteristics of the laboratory model of this computer have been quite satisfactory, as is seen in Fig. 11, where the linearity of the component circuits are shown. The 'Boxcar' and the phantastron circuits are quite linear and the maximum error in them is within $\pm 2\%$. The *FM* output p_1 varies from 0–20 Kc/s with $f_0 = 70$ Kc/s and is suitable to obtain 100 pulses for a gating pulse $f_7 = 5$ *m*sec and cos $\theta_j = \pm 1$. Assuming that 5 msec. corresponds to $f_j = 100$, there will be a single pulse output for $\cos\theta_j = \pm.01$; and for $f_j = 50\mu$ sec., corresponding to $f_j = 1$, there will be only one pulse for $\cos\theta_j = \pm 1$. Thus the accuracy in the multiplier would be about $\pm 1\%$; but this may be

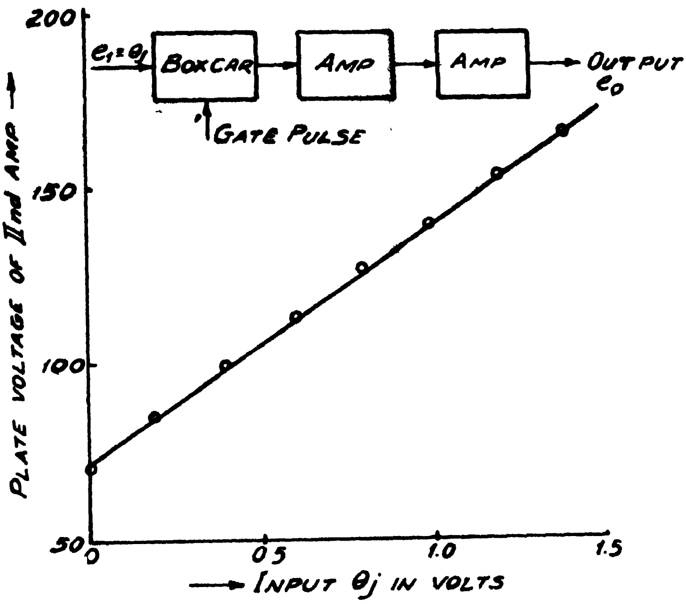

Fig. 11. *Linearity characteristics of the Component circuits in the Hybrid Computer.*
(*a*) Input θ_j vs. output voltages e_0 of the Boxcar and the associated amplifiers.

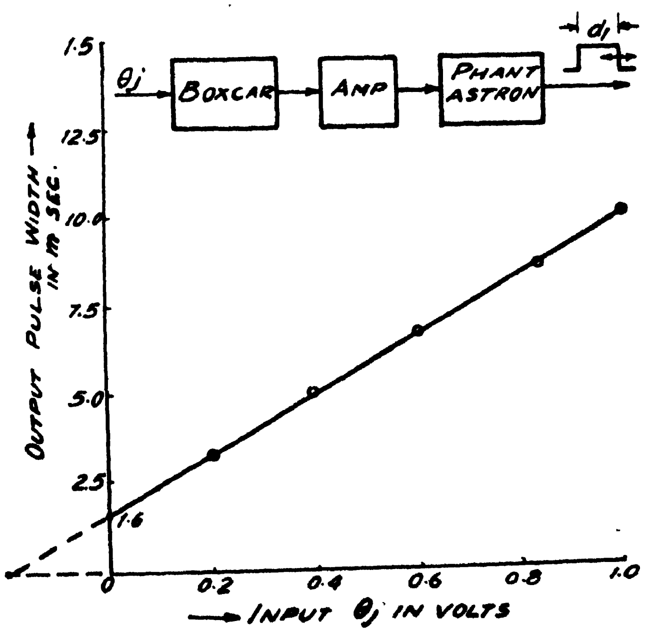

Fig. 11. (*b*) Variable of pulse width d_1 of the phantastron with θ_j
(minimum d_1 = 1.6 ms. for θ_j=0).

further improved if p_1 varies in a higher frequency range, say, from 0 200 Kc/s. The overall translator-multiplier characteristics are shown in Fig. 12 for some

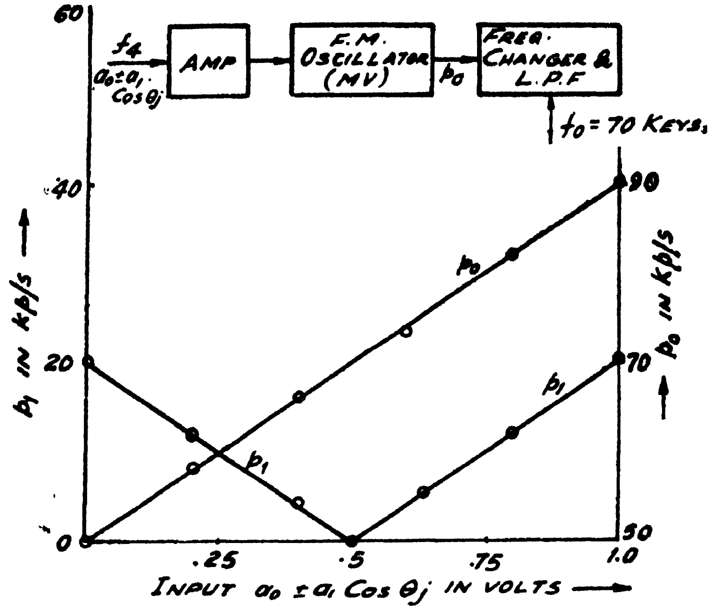

Fig. 11 (c) Variation of the frequency p_0 of the FM oscillator and the beat freq. $p_1 = (p_0 - f_0)$, with input $= (a_0 \pm a_1 \cos \theta_j)$.

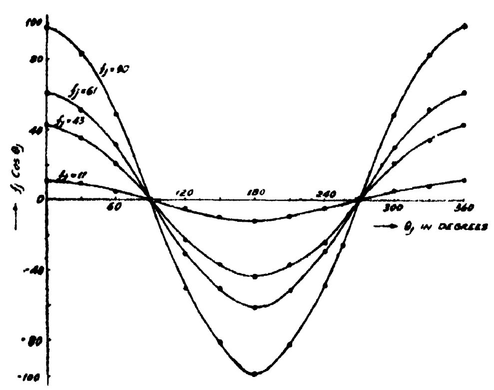

Fig. 12. Overall characteristics of the Hybrid Computer shown in Fig. 10. The counter outputs are for different θ_j in degrees for $f_j = 98$, 61, 43, and 11. Errors is ± 1.

values of f_j, and it is seen that the products $f_j \cos \theta_j$ are within ± 1 of their correct values.

The calibrated voltage inputs θ_j and f_j may be fed through push-button keys connected to a potential-divider chain. Two rows of keys, one for each digit in θ_j/f_j, may be coupled through an adding circuit to give the two-digit values of the inputs. It is also possible to feed the inputs through two dials and the digits stored in ring counters as is done in Fig. 9. The cathodes of the ring counters in Fig. 13 are connected to the adder through a suitable weighting network such

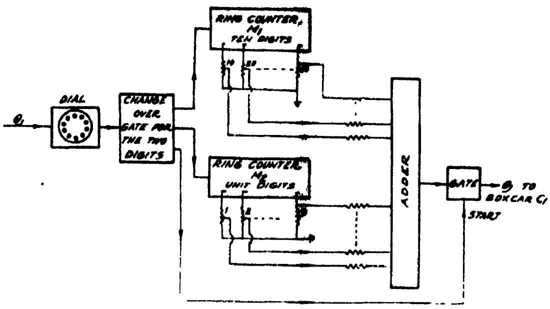

Fig. 13. Method of dialling the input θ_j to the Translation of Fig. 10.

that the added output is proportional to the dialled input θ_j. On completion of the storage (Flowers, 1951), a third gate feeds this added voltage θ_j to the translator in Fig. 10. At the end of each summing operation, it would be necessary to discharge the clamps C_1 and C'_2; this is done by using a recycling pulse generated from the trailing edge of the gate pulse f_5 or f_7. If the whole system is synchronised with 50 c/s mains, then a single operation would be complete within 20 msec. Thus it would be possible to perform about 3000 operations per minute if the inputs can be fed at such speeds. The speed is then mainly controlled by the input circuit and would be restricted to about 500 operations per hour using common telephone dials.

An extension to the two- and three- dimensional problems.

In many physical problems, it is necessary to evaluate the summation $\Sigma f_j \cos 2\pi (hx_j+ky_j+lz_j)$ or $\Sigma f_j \cos 2\pi(hx_j+ky_j)$ and the input θ_j to above computer has to be predetermined in terms of two or three-dimensional functions $(hx_j+ky_j+lz_j)$. If required, this may also be instrumented with circuits similar to those already discussed. Two such circuits for the two-dimensional case are shown in Fig. 14, which may be connected ahead of the relevant computers. The digital circuit of Fig. 14(a) is dial-controlled and uses the multiplier and adder similar to

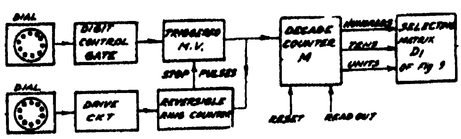

Fig. 14. Extension of the technique to two-dimensional problems.
(a) Digital multiplier—adder for fun tions $(hx+ky)$.

those of Fig. 9. The adder-counter M can now replace the digit-store M_1 and M_2 of Fig. 9. and the different digit signals (positive or zero voltages) may be directly

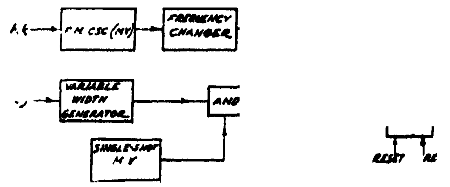

Fig. 14(b) Hybrid multiplier-adder for $(hx+ky)$.

fed to the selecting matrix D_1. The readout gate is operated after the required addition is completed in a manner similar to the generation of the start signal to MV_1 from T_3 of Fig. 9.

The hybrid circuit of Fig 14(b) uses the multiplier and adder of Fig. 10 and (hx_j+ky_j) is stored in the counter M. Since the input θ_j to the tranlator is an analogue voltage, the counter output is taken through a digital-to-analogue converter similar to that shown in Fig. 13. The dialling arrangement of Fig. 13 may now be used to feed h, k, x, y to the above auxiliary multiplier-adder.

CONCLUSIONS

Three simple and practical computing schemes for determining the Fourier coefficients have been studied, and the hybrid computer has been found to be sufficiently acurate (within about 1%) for general calculations. For higher acuracy and speed, the simplified digital computer may be used, although the speed is mainly dependent on the input circuit. The scheme with electromechanical switches is quite attractive and cheap, but careful maintenance of the equipment would be required for continuous operation. The electronic digital scheme uses about 700 diodes, 13 decade counters and associated control circuits for 3-digit values of θ_j and f_j, whereas for 2-digit values of the variables, 500 diodes and 10 counters are necessary. The hybrid scheme, using 5 gates, FM and Width-modulation circuits and controls, would require about 40 tubes, and a summing operation will be completed in 20msec. The values of θ_j and f_j may be fed through punched tapes or by simple dialling, and it will be possible to have about 500 operations per hour by using ordinary dials.

ACKNOWLEDGMENT

The authors record their thanks to Dr. G. B. Mitra for suggesting the problem and for valuable discussions; and also to Prof. H. Rakshit, D.Sc., F.N.I., for his kind interest in the work.

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